[Total No. of Questions - 9] [Total No. of Printed Pages - 3] (2125)

15318

B. Tech 7th Semester Examination

CMOS & VLSI Design (NS)

EC-415

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Attempt any one question:

1. (a) Explain VLSI design flow with flowchart describing various steps used in design process.

   (b) Explain in detail the Gate Array and Standard Cell based VLSI design. (20)

OR

2. (a) Derive the expression of drain current of NMOS transistor using gradual channel approximation.

   (b) For CMOS inverter derive expression of V_{IH}. Determine NM_H for symmetric operation. (20)

Attempt any one question:

3. (a) Describe with equations the extraction of parasitic capacitance of MOS transistor and interconnect.

   (b) Implement $f = \overline{(A + B + D)(C + E)}$ using static CMOS logic. Determine the W/L ratio of each MOSFET so that V_{OL} is always less than or equal to CMOS inverter. Draw the stick diagram. (20)

OR

[P.T.O.]

4. (a) Discuss cascading and charge sharing problem of basic dynamic CMOS logic. Implement the function $f = (\overline{A} + \overline{B} + \overline{D})(\overline{C} + \overline{E})$ using domino CMOS logic.

   (b) Define rise time, fall time and τ_{PLH} of inverter. Obtain equation of delay τ_{PHL} for CMOS inverter driving load C_L. (20)

Attempt any one question:

5. (a) Draw stick diagram and complete layout representing all layer for 2x1 multiplexer using CMOS logic.

   (b) Design 3-bit carry look-ahead adder and realize with dynamic CMOS logic. (20)

OR

6. (a) What is the Latch up problem that arises in CMOS' technology? Explain with analysis. How is it overcome?

   (b) Draw circuit of 2 phase clock generator. Draw stick diagram and explain operation of 4-bit dynamic shift register.

Attempt any one question:

7. (a) Draw logic diagram of CLB of FPGA having 4 input LUTs and describe its operation.

   (b) Implement following Boolean functions using PAL and PLA:

   f1(A, B, C, D) = Σm(0, 2, 6, 7, 8, 9, 12, 13, 14)

   f2(A, B, C, D) = Σm(2, 3, 8, 9, 10, 12, 13) (20)

OR

8. (a) What is the purpose of programmable interconnects? Describe array based and switch box based programmable wiring.

   (b) Explain difference between Sea-Of-Gate and standard cell. Draw layout of 2-input CMOS NOR gate using both approach. (20)

Attempt all questions:

9. (i) Write the threshold voltage equation for PMOS with body bias. Define parameters used in the equation.

   (ii) List the parasitic capacitances of MOS device. Are they constant? Why?

   (iii) Plot CMOS inverter transfer characteristics showing various region and status (off, triode or saturation) of PMOS and NMOS transistors in each region.

   (iv) Draw CMOS domino logic for realizing 3-input NOR gate.

   (v) Show the structure of 12-bit carry-bypass adder having 3 bypass stages.

   (vi) What are the factors that cause static power dissipation in the CMOS circuit?

   (vii) Draw NAND based CMOS SR latch.

   (viii) Distinguish between FPGA and CPLD.

   (ix) NMOS transistor has gate, drain and threshold voltages as V_G=3V, V_S=1.5V and V_T=0.7V. Neglecting body effect, determine its region of operation if (i) V_D=2V (ii)V_D=2.5V.

   (x) Realize 2-input NAND gate with CMOS logic.

(2×10=20)